JEDEC STANDARD

Electrically Erasable Programmable ROM (EEPROM) Program/Erase Endurance and Data Retention Stress Test

JESD22-A117C

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JEDEC Solid State Technology Association

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ELECTRICALLY ERASABLE PROGRAMMABLE ROM (EEPROM) PROGRAM/ERASE ENDURANCE AND DATA RETENTION STRESS TEST

(From JEDEC Board Ballot JCB-11-73, formulated under the cognizance of the JC-14.1 Subcommittee on Reliability Test Method and Packaged Devices.)

1 Scope

This stress test is intended to determine the ability of an EEPROM integrated circuit or an integrated circuit with an EEPROM module (such as a microprocessor) to sustain repeated data changes without failure (program/erase endurance) and to retain data for the expected life of the EEPROM (data retention). This Standard specifies the procedural requirements for performing valid endurance and retention tests based on a qualification specification. Endurance and retention qualification specifications (for cycle counts, durations, temperatures, and sample sizes) are specified in JESD47 or may be developed using knowledge-based methods as in JESD94.

This stress test does not replace other stress test qualification requirements. The program/erase endurance and data retention test for qualification and monitoring, using the parameter levels specified in JESD47, is considered destructive. Lesser test parameter levels (e.g., of temperature, number of cycles, retention bake duration) may be used for screening as long as these parameter levels have been verified by the device manufacturer to be nondestructive; this can be performed anywhere from wafer level to finished device.

2 Terms and definitions

2.1 EEPROM

A reprogrammable read-only memory in which the cells at each address can be erased electrically and reprogrammed electrically.

NOTE The term EEPROM in this document includes all such memories, including FLASH EEPROM integrated circuits and embedded memory in integrated circuits such as Erasable Programmable Logic Devices (EPLDs) and microcontrollers. Destructive-read memories such as ferroelectric memories, in which the read operation re-writes the data in the memory cells, are beyond the scope of this document.

2.2 Data pattern

The mix of 1s and 0s in the memory and their physical or logical positions.

NOTE A device may be single-bit-per-cell (SBC), meaning that one physical memory cell stores a “0” or a “1”, or multiple-bits-per-cell (MBC), meaning that one cell stores typically two bits of data: “00”, “01”, “10”, or “11”. In some MBC memories, the two bits represent logically-adjacent bit-pairs in each byte of data. For example, a byte containing binary data 10110001 would correspond to four physical cells with data 2301 in base-four logic. In other MBC memories, the two bits may represent bits in entirely different address locations. For an SBC memory a physical checkerboard pattern consists of alternating 0s and 1s, with each 0 surrounded by 1s on either side and above and below; a logical checkerboard pattern consists of data bytes AAH or 55H in which each 0 is logically adjacent to 1s. In some qualifications only logical positions may be known.

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2.3 Endurance

The ability of a reprogrammable read-only memory to withstand data rewrites and still comply with its specifications.

NOTE 1 EEPROM device specifications often require an erase step before reprogramming data; in this case a data rewrite includes both erase and programming steps, which together are called a program/erase cycle. Direct-write memories allow data to be written directly over old, without an erase; in this case the use of the generic term "program/erase cycle" will refer to a single rewrite with no erase. For SBC memories that require an erase step, one program/erase cycle consists of programming cells (typically to "0") and then erasing ("1"). For the comparable MBC case, a cycle would consist of programming cells (to "0", "1", or "2") and then erasing ("3").

NOTE 2 Endurance stressing consists of performing multiple rewrites in succession, and the data pattern or patterns for these rewrites must be chosen. There is no one data pattern or set of patterns that is worst-case for all failure mechanisms. For example, for floating-gate memories a fully-programmed pattern is worst-case for charge transfer, but a physical checkerboard pattern is worst-case for spurious programming of adjacent cells, and a mostly-erased pattern may be worst-case for mechanisms related to erase-preconditioning algorithms. For MBC memories, programming to the highest state is worst-case for charge transfer, but intermediate-state cells may experience more programming time and also have less sensing margin. Finally, in some memories, the margin of a cell is influenced by the data states of the physically adjacent cells.

2.4 Endurance failure

A failure that arises during endurance cycling.

NOTE 1 An endurance failure occurs if the device fails to complete the program or erase operations within the datasheet-specified times or if it fails to meet any of its other datasheet requirements as a result of program/erase cycling. A program operation that results in incorrect data being stored in the device counts as an endurance failure. However, if an error-management method such as an error-correction code is built into the device or specified to be applied by the system, then failure is taken to occur only if the error is not properly managed by the specified method.

NOTE 2 Certain products are specified to operate with either internal or external bad-block management system (BBM). When the BBM system detects an endurance failure it directs the data to another (spare) block and removes the address of the failing block from an appropriate address table. An endurance failure of such product is taken to occur when a pre-set number of spare blocks of the product had been consumed within that product datasheet specified cycle count.

NOTE 3 A number of distinct failure mechanisms are responsible for endurance failures, and in general these are accelerated in different ways by temperature and other adjustable qualification parameters. For example, in floating-gate memories failure may be caused by charge trapping (normally accelerated by lower temperatures) in the charge transfer dielectric or by oxide rupturing (normally accelerated by higher temperatures) in the transfer dielectric or in peripheral dielectrics.

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2.5 Failure

The loss of the ability of a component to meet the electrical or physical performance specifications that (by design or testing) it was intended to meet.

NOTE 1 The term *failure* is often qualified by an adjective describing the type of failure. For example, a component is a functional failure if it fails to function and a parametric failure if it functions but does not meet a datasheet specification for a parameter such as power consumption. Endurance and retention failures are defined in 2.4 and 2.7.

NOTE 2 Failures may be firm or transient. For the purpose of this standard, a firm failure is a component that fails sometime during a reliability stress and continues to fail at the final test at the end of that same stress. A transient failure is a component that fails during a reliability stress but passes in the final test at the end of that stress.

2.6 Retention

The ability of the EEPROM cell to retain data over time.

NOTE 1 The term data retention may refer to the ability of a device to retain data in the unbiased state, but the term will sometimes be used to include the ability to retain data under bias. The term "disturb" refers unambiguously to the ability of an EEPROM cell to retain data over time under bias. For example, read disturb refers to the ability of an EEPROM cell to retain data after being read a given number of times. A detailed discussion of disturbs is beyond the scope of this document.

NOTE 2 Retention stressing consists of writing a data pattern into a device and then verifying that the pattern is intact after a specified time at a specified temperature. There is no single data pattern that is worst-case for all retention mechanisms, cell designs, or process architectures. There are generally some failure mechanisms which primarily affect programmed cells and some which primarily affect erased cells, and there are also failure mechanisms which depend on the data in adjacent cells.

2.7 Retention failure

A change of stored data by one bit or more detected when the device is read according to data sheet specifications.

NOTE 1 If an error-management method such as an error-correction-code is built into the device or specified to be applied by the system, then failure is taken to occur only if the error is not properly managed by the specified method.

NOTE 2 A number of distinct failure mechanisms are responsible for retention failures, and in general these are accelerated in different ways by temperature and other adjustable qualification parameters. For example, in floating-gate memories, failure may occur due to defects that allow charge to leak through the transfer dielectric or by the detrapping of charge in the transfer dielectric; the former can be weakly accelerated or even decelerated by high temperature, and the latter can be highly temperature-accelerated.

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2.8 Uncorrectable bit-error rate (UBER)

A metric for data corruption rate, equal to the number of data errors per bit read after applying any specified error-correction method.

NOTE 1 The uncorrectable bit error rate is calculated from the following equation:

$$UBER = \frac{cumulative\ number\ of\ data\ errors}{cumulative\ number\ of\ bits\ read} \quad (1)$$

For non-error-corrected devices, any data bit in error counts as a data error. For error-corrected devices, any codeword or sector (as defined in the product data sheet) returning incorrect data after applying the specified error-correction scheme counts as a data error. Transient data errors, such as data errors that occur at a given program/erase cycle but not at later ones, are counted as data errors. Standard statistical confidence levels may be applied to the numerator.

The cumulative number of bits read is the sum of all bits of data read back from the device, with multiple reads of the same memory bit counting as multiple bits read. For example, if a 1-Gb device is read 10 times, then there would be 10 Gb bits read.

NOTE 2 Some devices may be specified to have a certain UBER value, and in this case the qualification must determine that the device meets the UBER specification. Section 5 discusses details regarding calculation of the UBER value.

3 Apparatus

The apparatus required for this test shall consist of a controlled temperature chamber capable of maintaining the specified temperature conditions to within ±5 °C. Sockets or other mounting means shall be provided within the chamber so that reliable electrical contact can be made to the device terminals in the specified circuit configuration. Power supplies and biasing networks shall be capable of maintaining the specified operating conditions throughout the test. Also, the test circuitry should be designed so that the existence of abnormal or failed devices will not alter the specified conditions for other units on test. Care should be taken to avoid possible damage from transient voltage spikes or other conditions that might result in electrical, thermal or mechanical overstress.

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4 Procedure

Qualification specifications, including those in JESD47, commonly require that some devices undergo both endurance stressing and, after being cycled, retention stressing. There may also be retention requirements for uncycled devices. Qualification specifications commonly call for endurance stressing to be performed at multiple temperatures within the datasheet range. Qualification specifications commonly call for retention stressing to be performed both at elevated temperatures, such as 125 °C, and room temperature. Figure 1 schematically illustrates the flow, with references to the paragraphs describing the procedure.

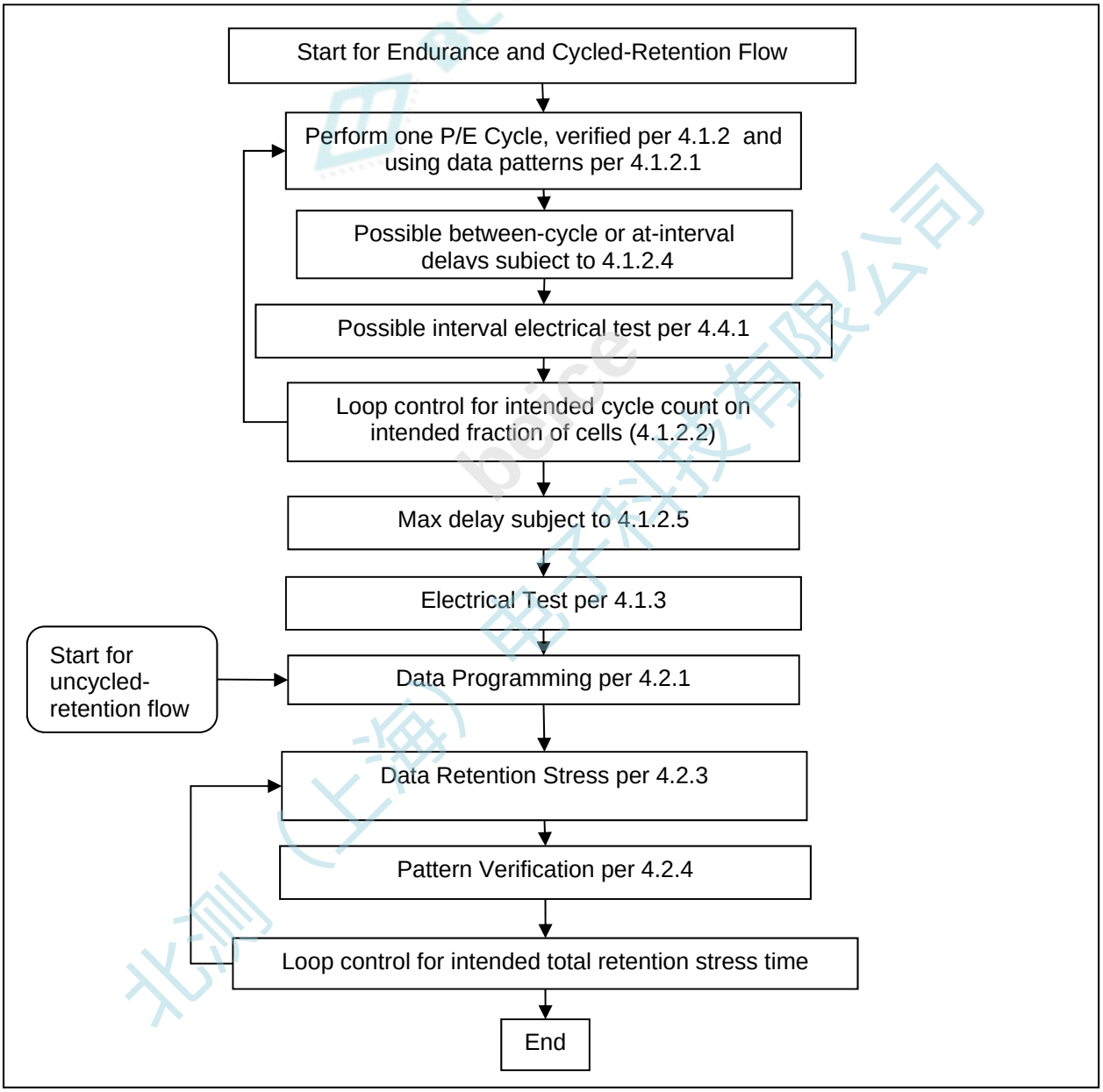

Figure 1 — Schematic Flow

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4.1 Program/erase endurance

4.1.1 Test setup

Devices shall be placed in the chamber so there is no substantial obstruction to the flow of air across and around each unit. The power shall be applied and suitable checks made to assure that all devices are properly energized. When special mounting or heat sinking is required, the details shall be specified in the applicable device specification and/or test specification.

4.1.2 Data cycling

Program and erase operations during the endurance test must be verified to have been properly executed per the device specification or the supplier's internal stress test specification (see 6).

4.1.2.1 Data patterns during cycling

The data pattern used for endurance cycling must be agreed upon between supplier and user, and the rationale documented. See 2.3 for a discussion of the tradeoffs involved in the selection of data pattern for cycling.

The purpose of many qualifications is to test the device for the broadest possible range of failure mechanisms. The broadest possible range of failure mechanisms can be detected when the data pattern includes the full range of logic levels and adjacency conditions that would occur in actual use. For example, this full range can be achieved if the following three conditions are met. First, the data in the memory cells is cycled between all available logic states in equal measure. For example, in an SBC memory half the cells would be programmed and half left erased in any one cycle, whereas in a 4-level-cell memory one-quarter of the cells would be written to each of the four available levels in any given cycle. Second, the positions of 1s and 0s are non-uniform, ideally quasi-random, so that all possible adjacency configurations are represented. For example, a data pattern consisting of a mix of bytes with data patterns 00H (zero zero hexadecimal), 55H, AAH, 33H, CCH, and FFH would create a wide range of adjacency patterns. Third, the data pattern in successive cycles is not the same, but rather follows a sequence. Best practice is to ensure, in this sequence, that some cells are written to all available logic states while other cells are re-written to the same logic state in every cycle. For example, in an SBC memory a byte that was cycled to AAH in even-numbered cycles and 5AH in odd-numbered cycles would have four cells that would be written to 0s and 1s in alternating cycles, two cells that are re-written to 0 in every cycle, and two cells that are re-written to 1 in every cycle.

In some knowledge-based qualifications, endurance tests may be defined for specific failure mechanisms. Such tests may use different data patterns from that described above, optimized to increase the sensitivity to the targeted mechanisms. Examples of acceptable data patterns for such purposes include a solid programmed pattern, checkerboard/inverse-checkerboard sequence, and checkerboard with subsequent filling-in of the pattern.

Some Flash EEPROM devices employ a built-in scrambling mechanism. When testing endurance of such devices, the scrambling mechanism should be enabled; disabling the scrambler for endurance cycling may stress the product beyond the stress a user may experience. A quasi-random pattern is best for testing endurance when employing scrambling.

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4.1.2 Data cycling (cont'd)

4.1.2.2 Fraction of cells to be cycled

Qualification specifications, whether from JESD47 or developed using knowledge-based methods (JESD94) will generally require that some fraction of the memory to be cycled to the maximum number of program/erase cycles specified in the device specification and other fractions to be cycled to lesser amounts. In large memories, it may take a prohibitively long time to cycle all cells to the maximum specification, and in knowledge-based qualifications it may be known that application use conditions do not require all cells to be so cycled. The actual fraction of cells cycled to 100% of the maximum specification, and the fraction cycled to other percentages of the specification, must be agreed upon between supplier and user and documented, along with the rationale for the chosen fractions.

4.1.2.3 Cycling conditions

The mode, voltages, temperature, and frequency of cycling should be agreed to between the supplier and user, and documented along with the rationale. Mode refers to different operational modes for program and/or erase, such as address, page, and block (or sector) program and erase modes. Voltages refer to all relevant supply voltages, including the logic-level supply and, if applicable, any high-voltage supply required for program or erase. Temperature refers to the temperature of the chamber in which the devices are cycled. Qualification specifications will often specify that some devices be cycled at low temperature and other devices be cycled at higher temperature. Frequency of cycling refers to the number of cycles performed per unit time.

4.1.2.4 Intentional delays between cycles

The degradation rate of EEPROM products may depend strongly on the cycling frequency. That is because some cycling-induced damage mechanisms exhibit partial recovery in between cycles; increasing the cycling rate may prevent that recovery and lead to early failures. Typical recoverable degradation mechanisms are the detrapping of charge trapped during cycling in the transfer-dielectric layer of floating gate devices, or detrapping of excess trapped charge in trapping-based non-volatile memories. Under user-mode application the product cycle count is spread over few years and the excess trapped charge may detrap between cycles, but if the product is run to maximum cycle count in few hours or days under qualification test mode, excess trapped charge will build up, leading to early product failure during the endurance cycling itself or in the following data retention test.

To avoid unrealistic stress during qualification testing the qualification flow may specify intentional delays to be added between cycles. This section describes methods for inserting relaxation delays during cycling and the rules and limitations that apply. The methods comprise:

(i) Cycling at elevated temperature (relaxation delays distributed evenly between cycles);
(ii) Cycling at elevated temperature at reduced cycle frequency (delays entered between each two cycles and / or between groups of cycles)
(iii) Ambient temperature cycling with high-temperature bake intervals inserted between groups of cycles.

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4.1.2 Data cycling (cont'd)

4.1.2.4 Intentional delays between cycles (cont'd)

The rule governing the insertion of cycling delays is that the resultant relaxation due to insertion of bake delays should not exceed the matching relaxation under user mode conditions. The total duration of inserted delays should be calculated from the difference between the intended use temperature and the delay temperatures, using the activation energy of the recovery mechanism. Combination of the above methods is allowed as long as the combination obeys this rule.

For cycling at elevated temperature according to method (ii), the supplier may specify that cycling shall not exceed certain number of cycles per day. During the rest of the day the devices may stay idle at the cycling temperature. The devices may be kept idle also at a different temperature, provided the total time at cycling temperature and the time at the idle temperature do not exceed together the matching cycling duration of the product at the intended use temperature (see example below).

To avoid exaggerated recovery effect towards end of cycling, cycling delays and/or bake intervals calculated for given group of cycles must be inserted at the beginning of each group of cycles. For example, if the supplier elects 4 even groups of cycles with even idling intervals between groups, and if the total allowed idle time at the idle temperature is calculated to be t_T, then fraction $t_T/4$ of the total idle time may be inserted at the beginning of the 2nd, 3rd, and 4th cycling groups. No relaxation delay is allowed at the end of the 4th group besides unavoidable logistical delay subject to the maximum specified in 4.1.2.5.

If the supplier elects to segment the cycling delays using non-even groups of cycles, the bake intervals shall be proportional to the fraction of cycles in the consecutive cycling group. The rationale for selecting non-even cycling groups is that bake delays at the early portion of the cycling flow are generally less effective for relaxing the device than delays towards the end of cycling, so the supplier may elect to skip early bake intervals and save in total stress test time.

Since the recovery effect may also depend on cell level; the supplier should specify the cell level used during delays between cycles. A cell level rotation among delays should also be used to simulate the usage conditions.

The supplier should document the method elected for inserting bake delays, report the data pattern used during delays, specify the recovery mechanism and provide the source for its activation energy. The supplier should document also the rationale for selecting the specific delays / bake intervals / temperatures during cycling.

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4.1.2 Data cycling (cont'd)

4.1.2.4 Intentional delays between cycles (cont'd)

Following are two examples illustrating how to select bake intervals.

Example 1 [method (ii)]:

Product cycle count = 10 k-cycle
Time for 10 k-cycle at intended application = 2 years = 17,520 h
User mode cycling temperature = 55 °C
Desired endurance qualification time = 10 days
Cycle time per day = 1 k-cycles @ 14 h
Qualification cycling temperature = 85 °C
Detrapping (relaxation) activation energy = 1.1 eV

What is the maximum allowed temperature during the idle period of 10 h per day?

a) 10 days x 14 hours of cycling per day at 85 °C are equivalent to 140 h x 26.1 = 3,652 h @ use temperature (Acceleration factor from 55 °C to 85 °C for Eaa = 1.1 eV is 26.1X)
b) Remaining equivalent user-mode cycling life is 17,520 h – 3,652 h = 13,868 h
c) The total idling time is 100 h
d) The thermal acceleration factor (A_T) from 100 hr to 13,868 hr is 138.68
e) To reach A_T = 138.6 with Eaa = 1.1 eV and T_{use} = 55 °C, T_{relax} = 102.6 °C

Answer: The maximum allowed temperature during the idle time is 102.6 °C. No delay is allowed on the last day after cycling besides the allowance for up to 12 h at cycling temperature per 4.1.2.5.

Example 2 [method (iii)]:

Product cycle count = 10 k-cycle
Time for 10 k-cycle at intended application = 2 years = 17,520 h
User mode cycling temperature = 35 °C
Qualification cycling temperature = 25 °C
Detrapping (relaxation) activation energy = 0.9 eV

Supplier wishes to insert bake intervals after 5 k-cycle and after 9 k-cycle. Bake temperature is 125 °C. What is the maximum allowed duration of each bake interval?

a) fraction of cycles of 2nd group is (9 k-cycle – 5 k-cycle)/10 k-cycle = 0.4
b) fraction of cycles of 3rd group is (10 k-cycle – 9 k-cycle)/10 k-cycle = 0.1
c) Thermal acceleration factor from 35 °C to 125 °C @ Eaa = 0.9 eV = X 2139
d) Total allowed relaxation time = 17,520 h / 2139 = 8.19 h
e) Maximum cycling delay before 2nd group = 8.19 x 0.4 = 3.28 h
f) Maximum cycling delay before 3rd group = 8.19 x 0.1 = 0.82 h

Answer: The maximum allowed bake interval @ 125 °C after 5 k-cycle is 3.28 h, and after 9 k-cycle it is 0.82 h.

NOTE Activation energies of in-cycling recovery mechanisms may vary between 0.8 eV and 1.2 eV according to technology and materials. See JEP122, 5.5 – 5.6.

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4.1.2 Data cycling (cont'd)

4.1.2.5 Delay at the end of endurance cycling

For cycling performed at elevated temperature, devices must not remain in the cycling chamber for more than 12 hours after completion of elevated-temperature cycling. For cycling at room temperature or below, any delay in the cycling chamber prior to removal of the devices must be counted in the overall 96-hour allowance discussed in 4.4.1. For devices with multiple regions that are independently cycled, these limits must be calculated starting from the time at which the first region finishes cycling. It may be necessary to stagger the cycling of the regions in order to meet these requirements. For example, if two regions are cycled, one to “n” cycles and one to “2n” cycles, then this may be accomplished by cycling the first region once and the second region twice, and then repeating this sequence a total of “n” times.

4.1.3 Electrical test verification

Verification of functional testing to the device specification after program/erase stressing shall be performed per 4.4.

4.2 Data retention

4.2.1 Data programming

Cycled devices completing the requirements of 4.1 and/or uncycled devices, as specified by the qualification specification, shall be programmed for subsequent retention testing. See 2.6 for a discussion of the tradeoffs involved in selecting the data pattern to be programmed. For qualifications whose purpose is to test the device for the broadest possible range of failure mechanisms, the memory should be written to all available logic states in equal measure, with the full range of adjacency configurations, as described in 4.1.2.1. Data should be written using the mode of programming specified on the datasheet.

In some knowledge-based qualifications, retention tests may be defined for specific failure mechanisms. Such tests may use different data patterns from that described above, optimized to increase the sensitivity to the targeted mechanisms. Examples of acceptable data patterns for such purposes include a solid programmed pattern, a solid erased pattern, a checkerboard pattern, and (for MBC) patterns with only some of the four logic levels represented. In such qualifications, data may also be written using a mode of programming that is different from that specified in the datasheet, to modify the margins of the cells and obtain additional acceleration.

The supplier shall document the method used and the rationale for that method.

4.2.2 Electrical testing and pattern verification (excluding any EEPROM program/erase testing)

Perform pattern verification and full functional testing to the applicable device specification, excluding any EEPROM program/erase testing. In some knowledge-based qualifications, special tests such as margin tests may be added to increase sensitivity to certain mechanisms, such as those which are poorly accelerated by temperature.

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4.2.3 Data retention stress

Qualification specifications (documented in JESD47 or in knowledge-based qualification plans based on JESD94) will call out retention durations and temperatures for both uncycled and cycled devices. Retention stress may consist of an unbiased bake (reference JESD22-A103C) or a biased life stress (reference JESD22-A108-B).

4.2.4 Electrical testing and pattern verification

Perform pattern verification and full functional testing to the applicable device specification. In addition, special tests such as margin testing may be used, as described in 4.2.2

4.3 Precautions

Precautions shall be taken to ensure that no devices can be damaged by thermal runaway and to preclude electrical damage. The test setup should be monitored initially and at the conclusion of a test interval to establish that all devices are being stressed to the specified requirements. The bias voltages and currents on each device shall be noted and corrected prior to further temperature exposure. If a device is not biased properly when checked at the conclusion of a test interval, it must be determined if the device has changed or if the test circuit has changed so that the validity of the data for qualification can be established.

4.4 Measurements

4.4.1 Electrical measurements

The electrical measurements shall be made at the completion of endurance and retention stresses, and may also be made at intervals (of retention cycle count and/or retention stress time) per the qualification specification. Interim read-points may be tested to less than full device specification values. Ideal practice for endurance testing is to verify the data written after every cycle, so that transient endurance failures are detected. If this is not practicable because of the time involved, then a method to account for such transient failures must be agreed upon between supplier and user (see 5.1). Final testing for endurance testing must test program/erase operation. Interim measurements in retention tests must not re-write the data. Interim and final electrical measurements shall be completed within 96 hours after removal of the devices from the specified test conditions. For endurance, this time includes any time spent in the cycling chamber following completion of cycling for any region of the device (see 4.1.2.5). For cycled units that subsequently enter retention stressing, the 96-hour limit applies to the entire delay time from completion of cycling on any region to the data programming step prior to data retention stress.

4.4.2 Required measurements

The electrical measurements shall consist of parametric, functional and timing tests specified in the applicable device specification.

4.4.3 Measurement conditions

Before removing the devices from the chamber, the ambient temperature shall be returned to room temperature while maintaining the specified voltages on the devices. Testing at room (or cold temperature if required per the device specification) shall be performed prior to testing at high temperature unless otherwise specified in the device specification.

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5 Failure criteria and calculation

A device is defined as a failure if the parametric limits are exceeded or if functionality cannot be demonstrated (e.g., data loss) as specified in the device specification. Any error management techniques that are part of the device specification should be applied in determining whether an event is to be considered a failure.

5.1 Handling of transient failures

For devices subject to transient failures, effort must be made to count all transient failures that occur in the stress. 4.4.1 requires electrical testing only at the end of stress, but this test will not detect earlier transient failures. Therefore, best practice is to test more frequently. For example, transient data errors are known to occur in some devices during endurance cycling, and the best practice is then to read back and verify the data after every cycle. If this is not possible, then some method must be used to estimate the occurrence of transient failures. This method must be documented and agreed upon between supplier and user (modeling and extrapolation methods beyond the scope of this standard may be needed). If a device is not subject to transient errors in a particular stress (such as is generally believed for retention stresses) then testing at the end of stress is sufficient.

For endurance cycling, an acceptable though conservative method is to scale the number of failures by the ratio of the number of cycles to the number of reads. For example, if data are read back and verified every 10^{th} cycle, one would multiply the number of failures detected by 10 to estimate the total number of failures that occurred. The rationale is that performing a read every 10^{th} cycle will detect only 10% of the failures if the failures are highly transient, occurring only in one cycle at the time of failure. If a qualification is to be performed to a stated upper confidence limit, then that confidence limit is to be applied before the multiplication. For example, if in the previous example the number of actual failures was zero but the upper confidence limit was 1, the total failures estimated with this method would be 10 rather than 1.

5.2 Separation of failures into data errors and device failures

Some devices may be specified to meet a UBER value. In that case, data-error failures will be separated from device failures. Device failures must meet the qualification criterion (such as the allowed number of failures specified in JESD47). Data errors must be within the product UBER specification. A device that fails is to be counted only as a single device failure, but under some circumstances a repeating data error should be counted multiple times (see 5.3).

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5.3 Calculation of UBER

Device qualification often contains endurance cycling operation followed by non-cycling stress such as a retention stress. In that case, the governing UBER definition of equation (1) may be restated as follows:

$$UBER = \frac{cumulative\ number\ of\ data\ errors}{\sum_{memory\ bits\ in\ sample}(endurance\ cycles \bullet reads\ per\ cycle + reads\ after\ cycling)} \quad (2)$$

The denominator is the number of bits read, starting from the first endurance cycle and extending through post-cycling stress (if such stress exists). The denominator is the sum over all memory bits in the devices sampled, each of which may in theory have a different value for endurance cycles, reads per cycle, and/or reads after cycling. The numerator is the number of data errors over the same time period (cycling followed by any post-cycling stress). As a general rule, a single memory location which has repeating data errors at multiple times during the stress shall be counted only once in the numerator, and reads of that location after the point of failure shall not be counted in the denominator. This general case follows from the assumption that locations with errors will be retired from use once an error occurs. A special case arises when the intended application will not retire such locations. In that case, a repeating data error must be counted multiple times, once for each repetition, and all reads of that location shall be included in the denominator. The number of times that an error should be counted depends on the intended application and must be agreed upon between supplier and user.

5.3.1 Calculation of UBER in the ideal case

At the end of an ideal endurance stress (data verified after every cycle), the numerator shall include all transient and firm errors from cycling, and the denominator shall have one read per cycle but no reads after cycling. Even if the endurance stress performs more than one read per cycle, the value used in equation (2) for reads per cycle shall be one unless the supplier states some other assumption and this is agreed upon with the user. At the end of a post-cycling stress, the numerator would include all errors during both cycling and the post-cycling stress, and the denominator would include both the cycling term and any reads after cycling. For a biased retention stress, as when read disturb is characterized, the reads after cycling shall be the actual number of reads performed. For an unbiased retention stress, the supplier may include some assumed non-zero number of reads after cycling (even if these reads were not actually performed during the stress) based upon the number of such reads expected in actual use over a time period believed equivalent to the retention stress. The rationale for any such assumption must be documented, and the assumption agreed to between supplier and user. For a device to be qualified to a UBER specification, separate UBER calculations must be performed at the end of endurance cycling and at the end of each post-cycling stress, and all such UBER values must meet the UBER specification. The statistical confidence limit, if any, applied to the numerator of equation (2) is to be stated and agreed to between supplier and user.

For example, if 100 devices of 1Gbit density were each subjected to 1000 endurance cycles with the data read once per cycle and no reads after cycling, then at the end of cycling the number of bits read would be 10^{14} ($=10^2*10^9*10^3$). The same denominator would be obtained if 10% of the memory bits were cycled 10,000 times and the remaining bits not cycled at all ($10\%x10^2*10^9*10^4$). Any single error during endurance cycling would result in a nominal UBER at the end of cycling of 10^{-14}, or a 90% upper confidence limit of $3.9x10^{-14}$.

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5.3.1 Calculation of UBER in the ideal case (cont'd)

If the devices then underwent an additional stress of 10,000 reads after cycling, then in the calculation of the UBER at the end of that post-cycling stress the denominator would increase by 10^{15} (10^2*10^9*10^4) to $1.1x10^{15}$. Then one single error either in cycling or in the post-cycling stress would result in a nominal UBER of $9x10^{-16}$, or a 90% upper confidence limit of $3.5x10^{-15}$. The UBER values calculated at the end of endurance and at the end of the post-cycling stress would both need to meet the UBER specification.

5.3.2 Calculation of UBER in other cases

The UBER calculated in the ideal case of 5.3.1 is considered here to be the true UBER for the device. If a qualification does not perform a read and data verify after every cycle, the calculation must be modified to estimate the true value as closely as possible. Therefore, the numerator is to consist of the total failures during the stress (transient failures estimated if necessary as described in 5.1) and the denominator is to include one read per cycle (unless otherwise specified per 5.3.1).

6 Summary

The following details shall be specified in the applicable device specification and/or the supplier's internal stress test specification, along with the rationale:

a) Special mounting, if applicable.

b) Test condition.

c) Biasing conditions.

d) Measurements before, at intermediate test points, (if applicable) and after test.

e) The maximum number of logic transitions in the memory cell, and the cycling patterns.

f) The period between program cycles.

g) Alternative program/erase procedures, requested by the EEPROM manufacturer, to guarantee the endurance requirement. This proposal must be approved by the user.

h) Data retention pattern, duration and temperature.

i) Cycling mode (e.g., sector mode, block mode, page mode).

j) Memory size under test.

k) Temperature during the program/erase stress.

l) Duration and temperature of any delays inserted at intermediate points during endurance stressing

m) Measured or presumed activation energy for selecting the relaxation bakes / cycling delays and selecting the data retention bake durations

n) Data pattern used for any delays inserted at intermediate points during endurance stressing

o) If UBER is reported – number of bit-reads in each experiment included in the cumulative bit-reads number, and method of extrapolation, if any.

p) Method used to account for transient endurance failures.

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Annex A (informative) Differences between JESD22 A117C and JESD22 A117B

This table briefly describes most of the changes made to entries that appear in this standard, JESD22-A117C, compared to its predecessor, JESD22-A117B (March 2009). If the change to a concept involves any words added or deleted (excluding typographical corrections), it is included.

A117C	A117B	Description
4.1.2.4	**4.1.2.4**	**Added 7th paragraph:** "Since the recovery…"
4.1.2.4	**4.1.2.4**	**In paragraph 8, first sentence added: "**report the data pattern used during delays"
6	**6**	**Summary:** Added new item (n), changed (n) to (o), and (o) to (p).

Annex B (informative) Differences between JESD22A117B and JESD22A117A

This table briefly describes most of the changes made to entries that appear in this standard, JESD22-A117B, compared to its predecessor, JESD22A117A (March 2006). If the change to a concept involves any words added or deleted (excluding typographical corrections), it is included.

A117B	A117A	Description
Preamble	**Preamble**	**Corrected** name of JEDEC governing subcommittee
2.4	**n/a**	**Failure:** New section with general definition of failure, definition of functional failure, parametric failure, firm failure and transient failure.
2.5	**2.4**	**Endurance failure:** Specifying endurance failure considering available bad-block management mechanism
2.6	**2.5**	**Retention:** definition of read disturb
2.8	**n/a**	**Uncorrectable bit error rate:** new definition
4.1.2.1	**4.1.2.1**	**Data pattern during cycling:** (1) Changed "2-bit per cell" to "4-level cell" (2) Added considerations for device with data scrambling mechanism.
4.1.2.4	**4.1.2.4**	**Intentional delays between cycles:** Section re-written. 2 examples added.
4.2.1	**4.2.1**	Reference to section 2.6 instead of 2.5
4.4.1	**4.4.1**	**Electrical Measurements**: (1) Added consideration for verifying endurance pattern each cycle, (2) corrected reference of 4.1.2.4 to 4.1.2.5
5	**5**	**Failure criteria and calculation:** Changed name of section
5.1	**n/a**	**Handling of transient errors:** New section
5.2	**n/a**	**Separation of failures to data errors and device failures:** New section
5.3	**n/a**	**Calculation of UBER:** New section
6	**6**	**Summary:** Add items (m), (n), (o).

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Annex C (informative) Differences between JESD22A117A and JESD22A117

This table briefly describes most of the changes made to entries that appear in this standard, JESD22A117A, compared to its predecessor, JESD22A117 (January 2000). If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

A117A	A117	Description
1	**1**	**Purpose:** Clarified relationship to JESD47. Deleted introductory background material (moved to and expanded in section 2).
2	**n/a**	**Terms, definitions, and technical background:** Added section. Contains expanded introductory background material and definitions of terms.
3	**2**	**Apparatus:** Specified ± 5°C temperature control
4	**3**	**Procedure:** Added flowchart. Replaced text requiring maximum-spec cycles with text referring to qualification plans that will specify the required cycling count.
4.1.2	**3.1.2**	**Data cycling:** Deleted sentences specifying "1" to "0" to "1" cycling and worst-case conditions.
4.1.2.1	**n/a**	**Data patterns during cycling:** Added section. Defines acceptable data patterns for single-level and multi-level memories (replacing "1" to "0" to "1" pattern in A117)
4.1.2.2	**n/a**	**Fraction of cells to be cycled:** Added section. Refers to JESD47 and JESD94 for requirements for the fraction of cells to be cycled.
4.1.2.3	**n/a**	**Cycling conditions:** Added section. Defines the cycling conditions that must be specified as part of a qualification report.
4.1.2.4	**n/a**	**Intentional delays between cycles:** Added section. Defines the acceptable methods for adding intentional delays between cycles.
4.1.2.5	**n/a**	**Delay at the end of endurance cycling:** Added section. Defines the acceptable delays between endurance cycling and subsequent testing
4.2.1	**3.2.1**	**Data programming:** Deleted requirement of "worst case pattern where all bits are programmed opposite to the intrinsic state." Added general recommendation for data pattern consisting of all data levels in equal measure, plus guidelines for special patterns for characterizing specific failure mechanisms.
4.2.2	**3.2.2**	**Electrical testing and pattern verification:** Added option for margin testing.
4.2.3	**3.2.3**	**Data retention stress:** Added reference to JESD22-A108-B for life stress retention evaluation. Added reference to JESD47 and JESD94 for specific retention stress temperatures and times.
4.2.4	**3.2.4**	**Electrical testing and pattern verification:** Added option for margin testing.
4.4.1	**3.4.1**	**Electrical measurements:** Added requirement that final endurance test include a program/erase cycle but that interim retention tests must not. Added requirement that any delays in the cycling chamber following completion of endurance stressing be counted towards the maximum allowable delay of 96 hours.
5	**4**	**Failure criteria:** Added stipulation that any error-management technique documented in the datasheet should be applied before determining that a device is a failure.
6	**5**	**Summary:** Added the following details that be specified: endurance cycling pattern; retention cycling pattern; and duration and temperature of any delays inserted into the cycling stress.

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Standard Improvement Form

JEDEC JESD22-A117C

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

_____

_____

_____

3. Other suggestions for document improvement:

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